TABLE V

Grid	n	Upper bound on $\underline{S}^2$	Lower bound on $\underline{S}^2$	Error in refinement near sing.	Error in refinement for infin.	Error in remaining region	Total error
1.2.2	47	55.74	52.02	0.541	1.740	1.441	3.722
1.2.4	57	55.24	52.35	0.465	1.137	1.286	2.888
1.∞.∞	32	54.75	52.76	0.183	0.549	1.259	1.991
2.4.4	156	54.31	53.04	0.193	0.754	0.323	1.270
2.4.8	192	54.10	53.22	0.176	0.403	0.296	0.876
2.∞.∞	77	53.90	53.41	0.044	0.146	0.293	0.483
4.∞.∞	215	53.71	53.57	0.013	0.052	0.074	0.139

For the problem with b = , a = 1, $\varepsilon_1 = 10\varepsilon_0$.

improve the solution on these two grids the best strategy is to place more refinements for the unbounded region, i.e., grids 1.2.4. and 2.4.8.

VI. Conclusion

In this paper some ideas on error assessment in the finite element method have been introduced for field problems. It has been shown how these ideas can be used to choose an optimum grid refinement pattern at a singularity and for an unbounded region. It has also been shown how the effect of arbitrarily assuming a zero solution outside some finite region can be assessed. By looking at element by element contributions to the error, those elements or groups of elements making major contributions to the error can be identified and singled out for refinement.

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Short Papers

Analysis of a Microwave FET Oscillator Using an Efficient Computer Model for the Device

ASHER MADJAR, MEMBER, IEEE

***Abstract*—This paper presents a time domain analysis of a microwave 10-GHz FET oscillator, which employs a practical and efficient computer model for the FET. Good agreement is demonstrated between the predicted and measured performance. A sensitivity analysis of the circuit is performed with respect to some of the FET parameters. This is useful information to estimate performance variation in production.**

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I. Introduction

In the last decade the GaAs MESFET has become an important and useful microwave device. Many microwave components can be built using this device—amplifiers, oscillators, switches, mixers, etc. To enable an accurate and efficient design of components using MESFET's it is useful to have a fast and reasonably accurate large signal model for the device. The basic model of Shockley [1] was shown to be invalid for GaAs short channel FET (modern microwave FET's belong to this category).

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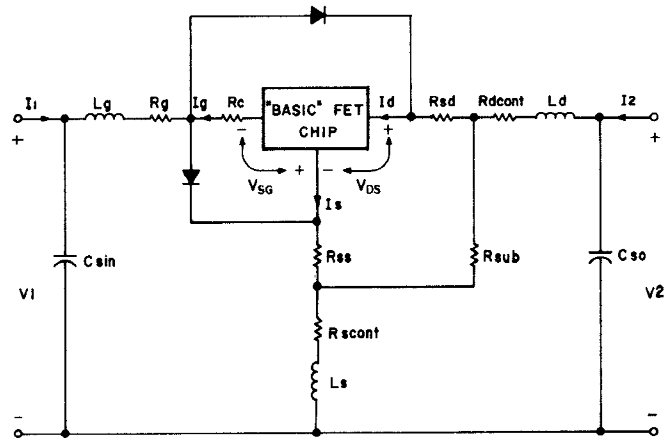

Fig. 1. Assembled MESFET chip model.

Thus, much work has been done in the last decade on FET modeling (see reference list of [2]). Most of this work is on numerical simulation, which is useful for understanding device operation; however, it is impractical for analysis and design of networks.

Recently a new model was developed by Madjar and Rosenbaum [2]–[4]. This model is almost entirely analytic, and thus very fast. It was shown to be practical and useful in the analysis of power amplifiers, oscillators, and frequency multipliers [2]. In this paper the new model is used to analyze a practical oscillator circuit suggested by Johnson [5]. Some of the predicted results are compared to the measured performance reported by Johnson. This way, two goals are achieved: 1) the usefulness and accuracy of the new model is demonstrated in a practical circuit; and 2) some of the properties of the particular oscillator are obtained. A brief description of the new model is given in Section II. The oscillator circuit to be analyzed is described in Section III. The simulation results are presented in Section IV.

II. The Computer Model

The new large signal computer model which is derived from basic principles is presented in detail in [2] and in a shorter form in [3], [4]. The region directly under the gate metalization is characterized by the mathematical relationship between the instantaneous currents and voltages

$$I_g = GVSG\frac{dV_{SG}}{dt} + GVDS\frac{dV_{DS}}{dt} \tag{1}$$

$$I_d = I_{\text{con}} + DVSG\frac{dV_{SG}}{dt} + DVDS\frac{dV_{DS}}{dt} \tag{2}$$

The currents and voltages are defined in Fig. 1. The conduction current, I_{con}, and the 4 capacitive coefficients ($GVSG, GVDS$, etc.) are functions of V_{SG}, V_{DS} and are calculated by the computer model. This representation is compatible with the state space approach in network analysis.

The complete equivalent circuit of the MESFET chip is given in Fig. 1. In addition to the basic FET characterized by (1) and (2), the model contains: R_{ss}, R_{sd}, bulk resistance of the regions between gate-source and gate-drain; and R_c, charging resistance of the channel. These quantities are calculated by the computer model. The other elements must be estimated by the user: L_g, L_s, L_d, wire bond inductances; C_{sin}, C_{so}, input and output stray capacitances; $R_g, R_{scont}, R_{dcont}$, contact resistances of the electrode metalization; and R_{sub}, parasitic resistance of the semi-insulating substrate. The two diodes represent the rectifying junctions drain-gate and source-gate, respectively.

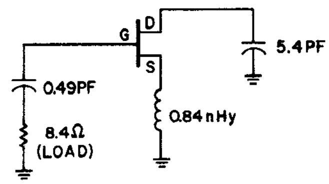

Fig. 2 Circuit diagram of the oscillator

III. The Oscillator Circuit

The FET oscillator that was analyzed is the one suggested by Johnson [5]. Its ac circuit is given in Fig. 2 (the component values correspond to a 10-GHz oscillation frequency). The figure does not include the biasing arrangement. The device used is a Texas Instruments FET in a coaxial package. Its equivalent circuit is as shown in Fig. 1 with the addition of an inductance in series with the gate and drain ports. Johnson has calculated by curve fitting methods the values of the parasitic elements in the equivalent circuit. These values were used in our simulation.

The important device parameters used in the simulation are: doping level, 10^{17} cm^{-3}; gate length, 1.2 μm; gate width, 600 μm; and epitaxial layer thickness, 0.3 μm. To prevent long transient times before steady-state is reached (and the accompanying long computation times), RF chokes and bypass capacitors are to be avoided in the simulated circuit. To achieve this, two changes were made in the circuit of Fig. 2: 1) the 5.4-pF capacitor was merged with the additional parasitic drain inductance to a single inductance; 2) the series RC combination in the gate was replaced by its parallel equivalent. Due to these changes, steady state was obtained in less than 15 cycles of the fundamental frequency.

The state equations of the oscillator circuit were derived, and their solution in the time domain was obtained by means of a standard IBM routine, RKGS, which employs the Runge–Kutta method. The waveforms, thus obtained, were Fourier analyzed by the IBM routine FORIT, yielding the frequency domain properties of the oscillator.

IV. Simulation Results

In this section the results of the 10-GHz oscillator circuit simulations are presented. The simulations were performed for a dc drain voltage of $V_{DS} = 8$ V and several values of gate voltage V_{SG} (corresponding to different values of dc current I_D). Fig. 3 shows the oscillator fundamental output power versus the dc current. The measured curve is from Johnson [5], who realized the 8.4-Ω load (Fig. 2) by a coaxial transformer from 50 Ω. This transformation is accompanied with some circuit loss. This loss is accounted for in the simulation by an additional resistance of 21 Ω in parallel with the 8.4-Ω load (total load resistance, 6 Ω). This value of resistance is reasonable (approximately 25-percent power loss), and gives the best fit to the experimental curve in Fig. 3. Obtaining each data point in Fig. 3 involves one full run of the computer program. The exectution time for each run is approximately 30 s on a CDC 6600 computer.

The harmonic content of the output voltage waveform was determined from the Fourier analysis. Typically, the second harmonic level is at least 15 dB below the fundamental, and the third harmonic level is at least 27 dB below the fundamental. This good spectral purity (with no high-Q resonant circuits) is

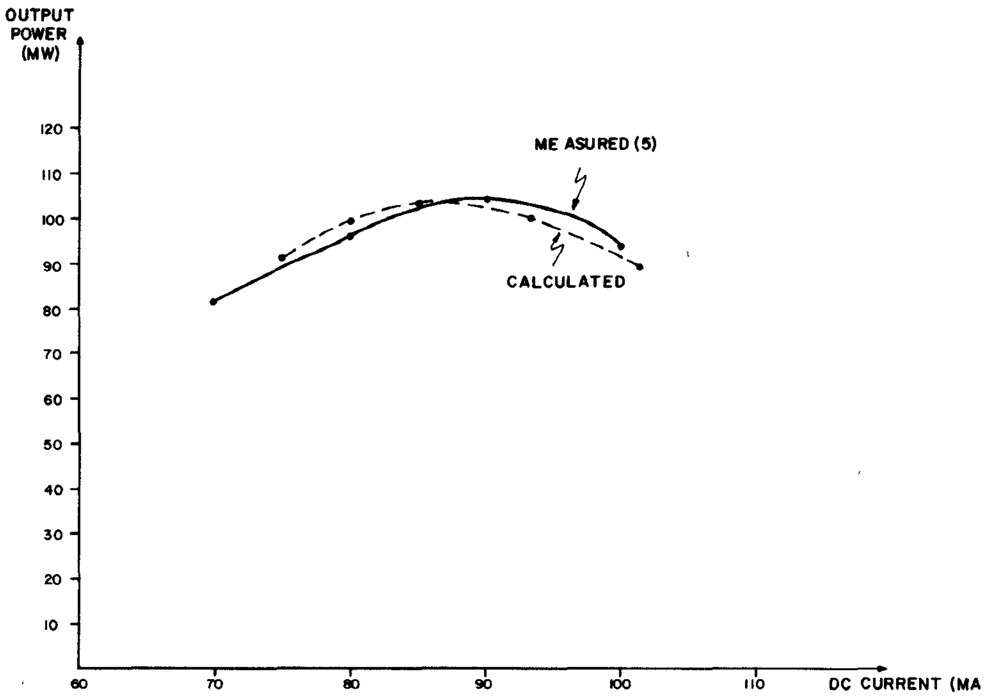

Fig. 3. Measured and calculated output power of the oscillator

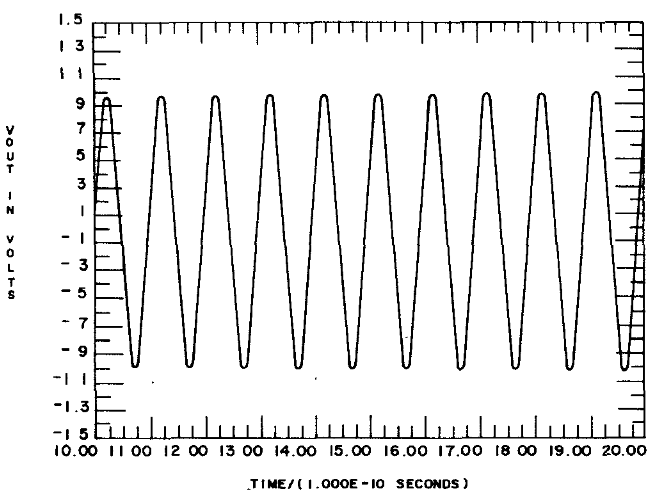

Fig. 4. Output voltage waveform.

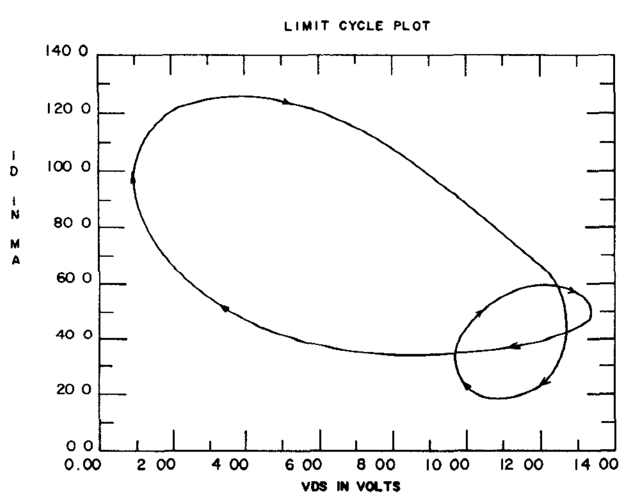

Fig. 5. Limit cycle plot.

probably due to the inability of the device to support such high frequencies. Fig. 4 presents the output voltage waveform in steady-state for one of the simulation runs. The good spectral purity is clearly evident.

Fig. 5 is a limit cycle plot. It shows the functional relationship between the drain current and voltage over one full cycle in steady state. The arrows indicate the direction of increasing time.

To test the sensitivity of this oscillator to the key device parameters two additional simulations were performed for a dc current of 85 mA. In one simulation the doping level was changed to $9.5 \cdot 10^{16}$ cm^{-3} (5-percent decrease). The resulting output power is 101 mW (compared to 104 mW in Fig. 3), namely a decrease of about 3 percent. So the sensitivity of the output power to the doping level is not large. In the second simulation the epitaxial layer thickness was changed to 0.29 μm (3-percent decrease). The resulting output power is 89 mW, namely a decrease of 15 percent!

V. Conclusions

A practical FET microwave oscillator circuit was analyzed by the use of a new large signal model for the FET. Some of the simulation results were compared to published experimental data, and were in good agreement. The properties of the oscillator were investigated, and were found to be well predicted by the model.

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